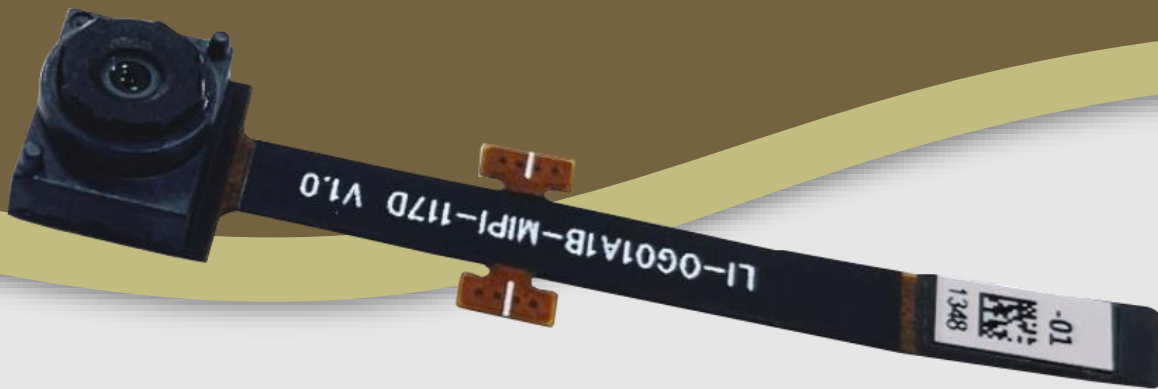




LI-OG01A1B-MIPI-117D-AR



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INTRODUCTION

The LI-OG01A1B-MIPI-117D-AR is equipped with OMNIVISION 1/5" 1.3MP backside-illuminated (BSI) global shutter image sensor OG01A1B which combines PureCel® Plus-S pixel technology and Nyxel® near-infrared (NIR) technology to enable optimal performance and precision. This camera outputs 8-bit / 10-bit RAW data.

SPECIFICATIONS

Sensor	OMNIVISION b&w CMOS 1.3MP Image Sensor OG01A1B
Optical Format	1/5"
Resolution	1280 (H) x 1024 (V) (active pixels)
Pixel Size	2.2 x 2.2 μ m
Shutter	Global shutter
Output Format	8-bit / 10-bit RAW data
Color / Mono	Monochrome
Maximum Frame Rate	120 fps @ 1280 x 1024 240 fps @ 640 x 480
Interface	2-lane MIPI CSI-2
Power Requirements	- Active: 184 mW @ 120 fps - XSHUTDOWN: 1 μ A
Operating Temp	-30°C ~ +85°C junction temp
Storage Temp	-40°C ~ +125°C ambient temp
Weight	~ 0.38 g
Part#	LI-OG01A1B-MIPI-117D-AR

APPLICATIONS

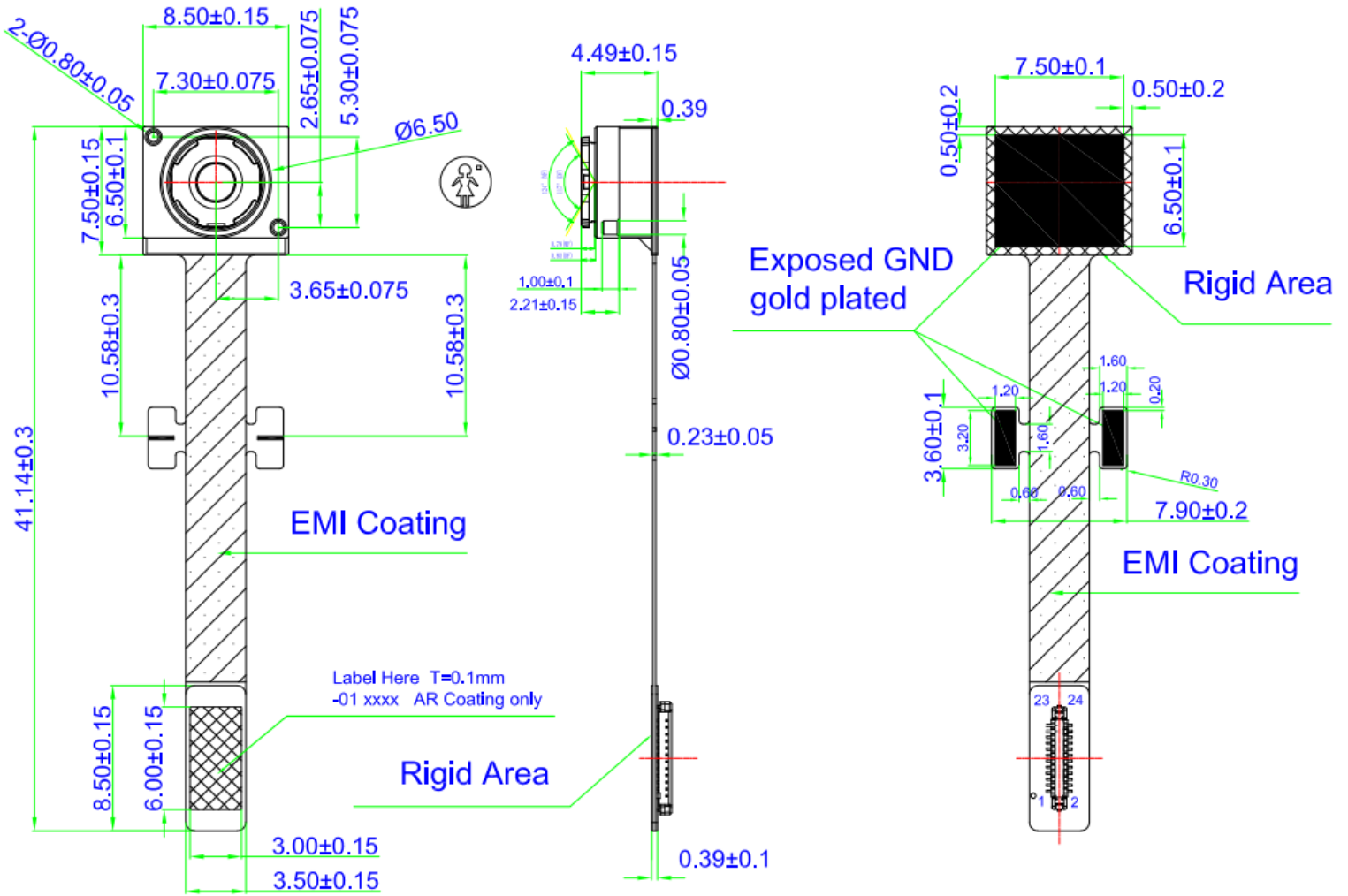
- Biometric Authentication
- Machine Vision
- Drones
- Industrial Automation
- 3D Imaging
- AR / VR
- Industrial Bar Code Scanning
- Gaming

LENS SPECIFICATIONS

Focusing Range	20 cm ~ Infinity
Focal Length	1.45 mm
Aperture, F/#	2.2
IR Filter	Not included
Field of View (FOV)	117° diagonal
	95° horizontal
	78° vertical
TV Distortion	< -13%



DIMENSIONS



NOTE:

1. Basic tolerance: ± 0.1 mm
2. Label with "*": important dimension

Unit: mm

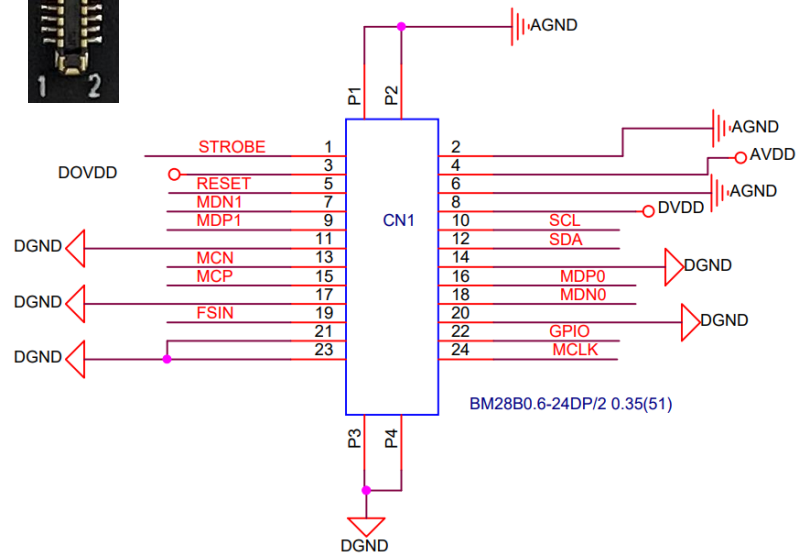
PIN ASSIGNMENT

NO.	Name	Type	Description
1	STROBE	Output	Strobe output
2	AGND	Ground	Ground for analog circuit
3	DOVDD	Power	Power for I/O circuit
4	AVDD	Power	Power for analog circuit
5	RESET	Input	XSHUTDOWN (active low)
6	AGND	Ground	Ground for analog circuit
7	MDN1	Output	MIPI TX data lane negative output (MC1C of CPHY)
8	DVDD	Power	Power for digital circuit
9	MDP1	Output	MIPI TX data lane positive output (MC1B of CPHY)
10	SCL	Input	SCCB clock
11	GND	Ground	Ground
12	SDA	I/O	SCCB data

NO.	Name	Type	Description
13	MCN	Output	MIPI TX clock lane negative output (MC1A of CPHY)
14	DGND	Ground	Ground for I/O circuit
15	MCP	Output	MIPI TX clock lane positive output (MC0C of CPHY)
16	MDP0	Output	MIPI TX data lane positive output (MC0A of CPHY)
17	DGND	Ground	Ground for I/O circuit
18	MDN0	Output	MIPI TX data lane negative output (MC0B of CPHY)
19	FSIN	I/O	FSIN I/O
20	DGND	Ground	Ground for I/O circuit
21	DGND	Ground	Ground for I/O circuit
22	GPIO	I/O	General purpose I/O
23	DGND	Ground	Ground for I/O circuit
24	MCLK	Input	System input clock

INTERFACE

- Connector Part#: BM28B0.6-24DP/2 0.35(51)
- Number of Positions: 24
- Pitch: 0.35 mm
- Number of Rows: 2



● REVISION HISTORY

Revision	Description	Release Date
1.0	First release.	01 Jul 2022

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