



LEOPARD IMAGING INC

# LI-V024M-PAR

## Data Sheet

### Key Features

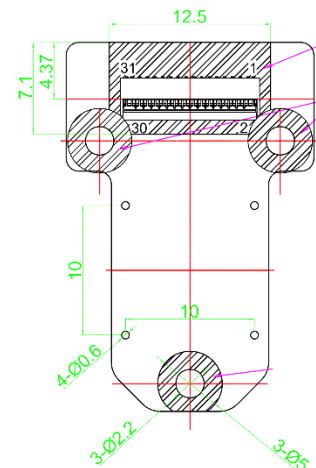
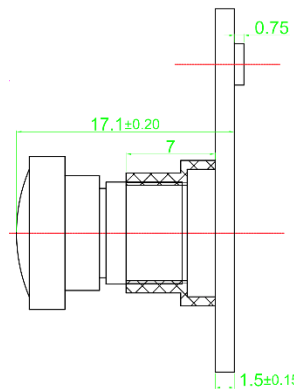
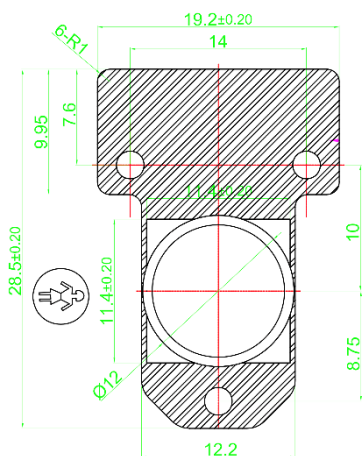
- ON SEMI Wide-VGA CMOS Digital Image Sensor MT9V024
- Optical format: 1/3"
- Active pixels: 752H x 480V
- Pixel size: 6.0 um x 6.0 um
- Global shutter
- RAW Data Output
- Monochrome camera
- Support 752 x 480 @ 60 fps
- Parallel interface
- Module Size: 28.5mm x 19.2mm
- Weight: 2 g
- Part#: **LI-V024M-PAR**



### Lens Spec

- Part#: YT-6007-H1
- Focusing range: 20cm to Infinity
- Focal Length: 1.3 mm
- Aperture, F/#: 2.0
- FOV (H): 170°
- Distortion: < -110%
- Mount: M8 x P0.5

### Dimensions



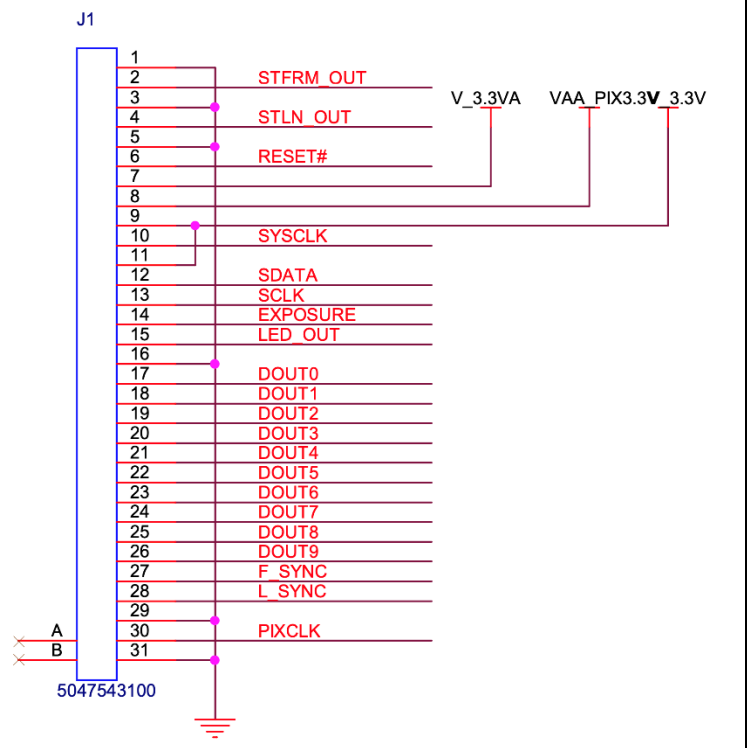
Leopard Imaging Inc.

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## Pin Assignment

### Interface J1:

- Part#: 5047543100
- Number of Positions: 31
- Pitch: 0.30 mm
- FFC, FCB Thickness: 0.20mm



## Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
$V_{SUPPLY}$	Power supply voltage (all supplies)	-0.3	4.5	V
$I_{SUPPLY}$	Total power supply current	-	200	mA
$I_{GND}$	Total ground current	-	200	mA
$V_{IN}$	DC input voltage	-0.3	$V_{DD} + 0.3$	V
$V_{OUT}$	DC output voltage	-0.3	$V_{DD} + 0.3$	V
$T_{STG}^{Note}$	Storage temperature	-50	+150	°C

Note: This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



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## DC Electrical Characteristics Over Temperature

VPWR = 3.3V ±0.3V; TJ = -40°C to +105°C; Output Load = 10pF; Frequency 13 MHz to 27 MHz; LVDS off

Symbol	Definition	Condition	Min	Typ	Max	Unit
V <sub>IH</sub>	Input HIGH voltage		V <sub>PWR</sub> - 1.4	-		V
V <sub>IL</sub>	Input LOW voltage			-	1.3	V
I <sub>IN</sub>	Input leakage current	No pull-up resistor; V <sub>IN</sub> = V <sub>PWR</sub> or V <sub>GND</sub>	-5	-	5	μA
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -4.0mA	V <sub>PWR</sub> - 0.3	-	-	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 4.0mA	-	-	0.3	V
I <sub>OH</sub>	Output HIGH current	V <sub>OH</sub> = V <sub>DD</sub> - 0.7	-11	-	-	mA
I <sub>OL</sub>	Output LOW current	V <sub>OL</sub> = 0.7	-	-	11	mA
I <sub>PWRA</sub>	Analog supply current	Default settings	-	12	20	mA
I <sub>PIX</sub>	Pixel supply current	Default settings	-	1.1	3	mA
I <sub>PWRD</sub>	Digital supply current	Default settings, C <sub>LOAD</sub> = 10pF	-	42	60	mA
I <sub>LVDS</sub>	LVDS supply current	Default settings with LVDS on	-	13	16	mA
I <sub>PWRA</sub> Standby	Analog standby supply current	STDBY = V <sub>DD</sub>	-	0.2	3	μA
I <sub>PWRD</sub> Standby Clock Off	Digital standby supply current with clock off	STDBY = V <sub>DD</sub> , CLKIN = 0 MHz	-	0.1	10	μA
I <sub>PWRD</sub> Standby Clock On	Digital standby supply current with clock on	STDBY = V <sub>DD</sub> , CLKIN = 27 MHz	-	1	2	mA

## DC Electrical Characteristics

VPWR = 3.3V ±0.3V; TA = Ambient = 25°C

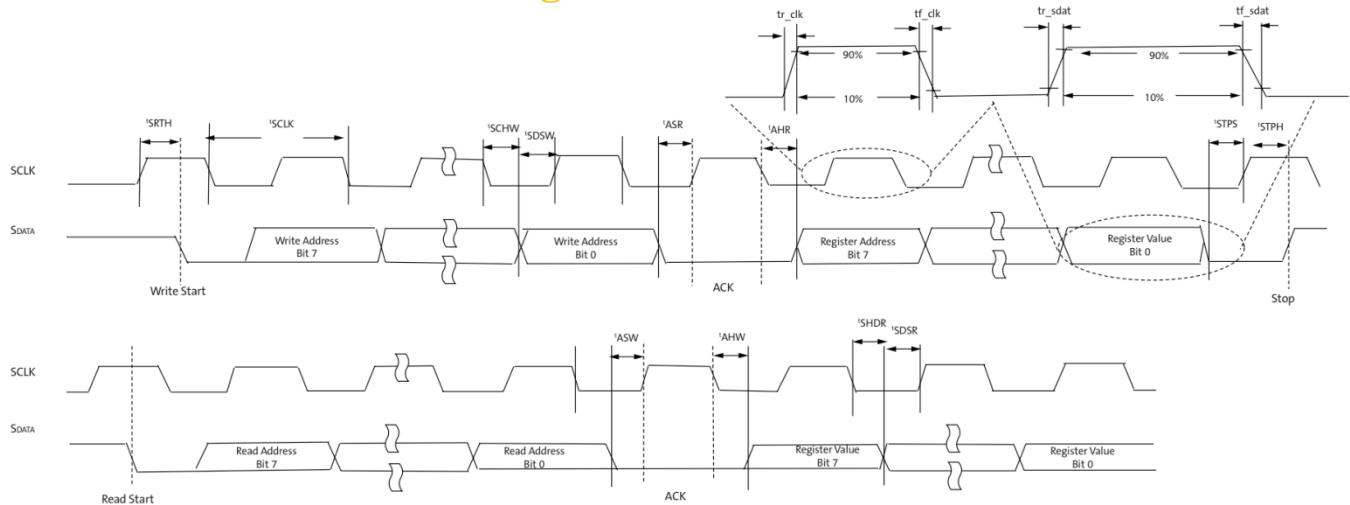
Symbol	Definition	Condition	Min	Typ	Max	Unit
LVDS Driver DC Specifications						
V <sub>OD</sub>	Output differential voltage	R <sub>LOAD</sub> = 100 Ω ± 1%	250	-	400	mV
DV <sub>OD</sub>	Change in V <sub>OD</sub> between complementary output states		-	-	50	mV
V <sub>OS</sub>	Output offset voltage		1.0	1.2	1.4	mV
DV <sub>OS</sub>	Pixel array current		-	-	35	mV
I <sub>OS</sub>	Digital supply current			±10	mA	
I <sub>OZ</sub>	Output current when driver is tri- state			±1	μA	
LVDS Receiver DC Specifications						
V <sub>IDTH+</sub>	Input differential	V <sub>GPD</sub>   < 925mV	-100	-	100	mV
I <sub>in</sub>	Input current		-	-	±20	μA



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## Two-Wire Serial Bus Timing



Test Conditions: 25°C, 26.67 MHz, and 3.3V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t^{\text{SCLK}}$	Serial interface input clock frequency				400	kHz
$t^{\text{SCLK}}$	Serial Input clock period				2.5	$\mu$ sec
	SCLK duty cycle	When active	40	50	60	%
$t^{\text{r\_sclk}}$	SCLK rise time			165		ns
$t^{\text{f\_sclk}}$	SCLK fall time			6		ns
$t^{\text{r\_sdat}}$	$S_{\text{DATA}}$ rise time	1.5 k $\Omega$ pull-up		180		ns
$t^{\text{f\_sdat}}$	$S_{\text{DATA}}$ fall time			9		ns
$t^{\text{SRTS}}$	Start setup time	WRITE/READ	148	150	167	ns
$t^{\text{SRTH}}$	Start hold time	WRITE/READ	36.9	36	37.6	ns
$t^{\text{SDSW}}$	$S_{\text{DATA}}$ setup	WRITE	0	5	12	ns
$t^{\text{SDHW}}$	$S_{\text{DATA}}$ hold	WRITE	1.3	36	37	ns
$t^{\text{ASW}}$	ACK setup time	WRITE	146	146	148	ns
$t^{\text{AHW}}$	ACK hold time	WRITE	98.9	107	144	ns
$t^{\text{STPS}}$	Stop setup time	WRITE/READ		624		ns
$t^{\text{STPH}}$	Stop hold time	WRITE/READ		1.61		ns
$t^{\text{ASR}}$	ACK setup time	READ	192	228	229	ns
$t^{\text{AHR}}$	ACK hold time	READ	247	284	287	ns
$t^{\text{SDSR}}$	$S_{\text{DATA}}$ setup	READ	654	655	690	ns
$t^{\text{SDHR}}$	$S_{\text{DATA}}$ hold	READ	560	595	596	ns
CIN_SI	Serial interface input pin capacitance			3.5		ns
CLOAD_SD	$S_{\text{DATA}}$ max load capacitance			15		ns
RSD	$S_{\text{DATA}}$ external pull-up resistor			1.5		k $\Omega$



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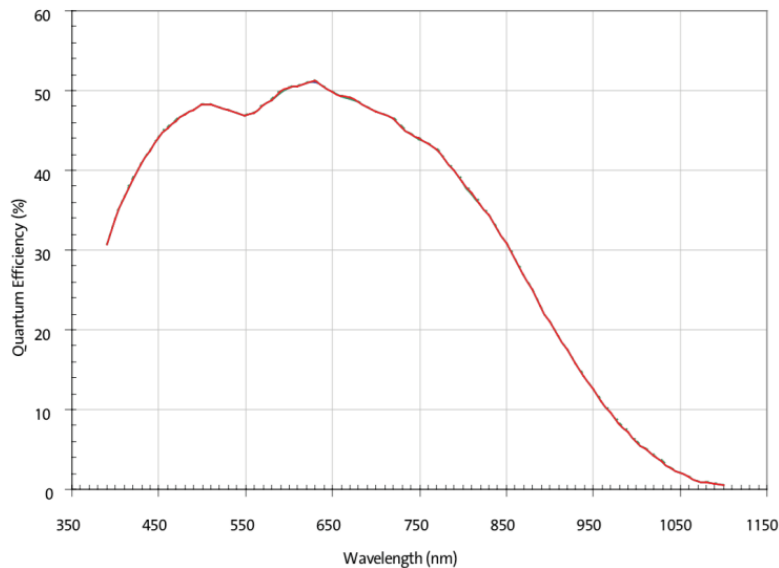
## AC Electrical Characteristics

VPWR = 3.3V ±0.3V; T<sub>J</sub> = -40°C to +105°C; Output Load = 10pF

Symbol	Definition	Condition	Min	Typ	Max	Unit
SYSCLK	Input clock frequency		13.0	26.6	27.0	MHz
	Clock duty cycle		45.0	50.0	55.0	%
t <sub>R</sub>	Input clock rise time		-	3	5	ns
t <sub>F</sub>	Input clock fall time		-	3	5	ns
t <sub>PLH<sub>P</sub></sub>	SYSCLK to PIXCLK propagation delay	C <sub>LOAD</sub> = 10pF	4	6	8	ns
t <sub>PD</sub>	PIXCLK to valid D <sub>OUT</sub> (9:0) propagation delay	C <sub>LOAD</sub> = 10pF	-3	0.6	3	ns
t <sub>SD</sub>	Data setup time		14	16	-	ns
t <sub>HD</sub>	Data hold time		14	16		
t <sub>PFLR</sub>	PIXCLK to LV propagation delay	C <sub>LOAD</sub> = 10pF	5	7	9	ns
t <sub>PFLF</sub>	PIXCLK to FV propagation delay	C <sub>LOAD</sub> = 10pF	5	7	9	ns

## Spectral characteristics

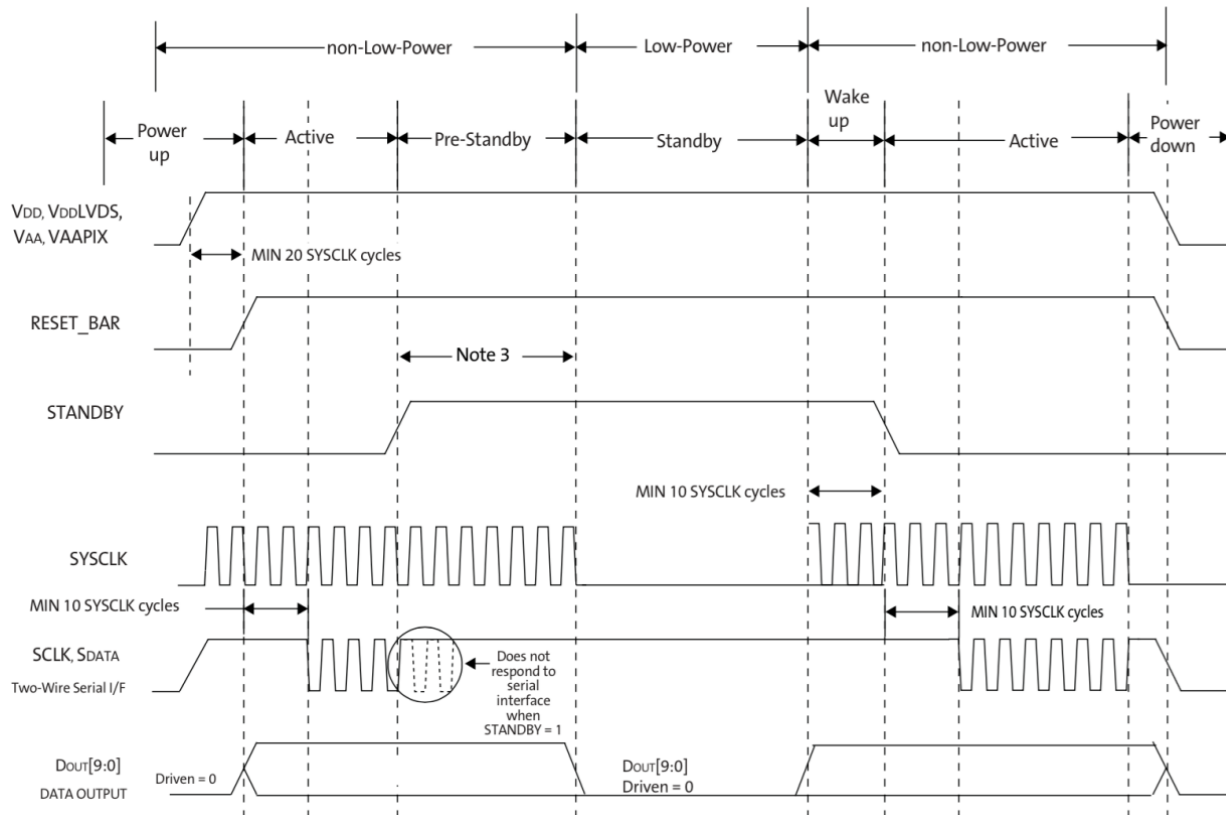
Typical Quantum Efficiency—Monochrome



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## Power-up, Reset, Clock, and Standby Sequence



- Note: 1. All output signals are defined during initial power-up with RESET\_BAR held LOW without SYSCLK being active. To properly reset the rest of the sensor, during initial power-up, assert RESET\_BAR (set to LOW state) for at least 750ns after all power supplies have stabilized and SYSCLK is active (being clocked). Driving RESET\_BAR to LOW state does not put the part in a low power state
2. Before using two-wire serial interface, wait for 10 SYSCLK rising edges after RESET\_BAR is de-asserted.
3. Once the sensor detects that STANDBY has been asserted, it completes the current frame readout before entering standby mode. The user must supply enough SYSCLKs to allow a complete frame readout.
4. In standby, all video data and synchronization output signals are driven to a low state.
5. In standby, the two-wire serial interface is not active.



## Revision History

Revision	Description	Release Date
1.0	First Release	15. Mar. 2020



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