LEOPARD IMAGING INC

LI-APOLLO-ADP-AR023Z-YUV Data Sheet

Key Features

- Compatible with Intel Apollo Processor board
- MIPI interface
- YUV output without compression
- Color sensor
- Built in AP0202 ISP
- Built in Parallel-to-MIPI Bridge
- Support two cameras
- Provide customization services
- Weight: 18 g
- Part#: LI-APOLLO-ADP-AR023Z-YUV

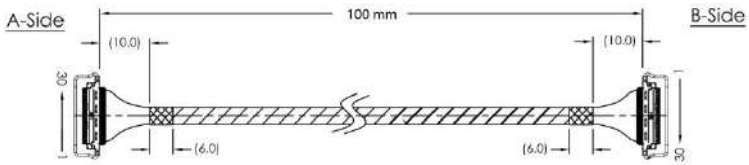
Lens Spec

- Model: M13B0618WR5
- Focal length: 6.0 mm
- Aperture, F/#: 1.8
- Built in 650nm IR cut filter
- FOV (D/H/V): 69° / 58° /31°
- IRIS: Fixed
- Mount: M12 x 0.5 – 6g

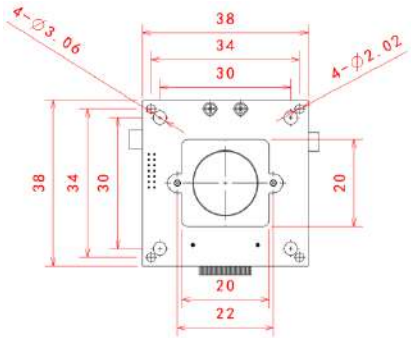
BOM

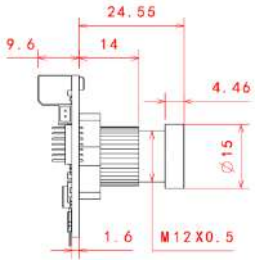
#	Items	QTY
1	LI-AR023Z-YUV-MIPI	1
2	FAW-1233-01 cable	1
3	LI-APOLLO-ADP	1

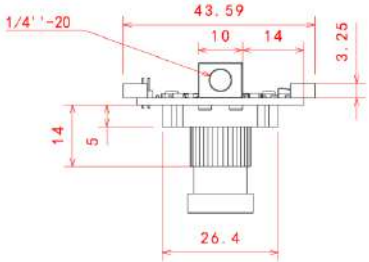
Dimensions (FAW-1233-01)

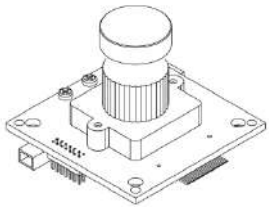


Dimensions (LI-AR023Z-YUV-MIPI)









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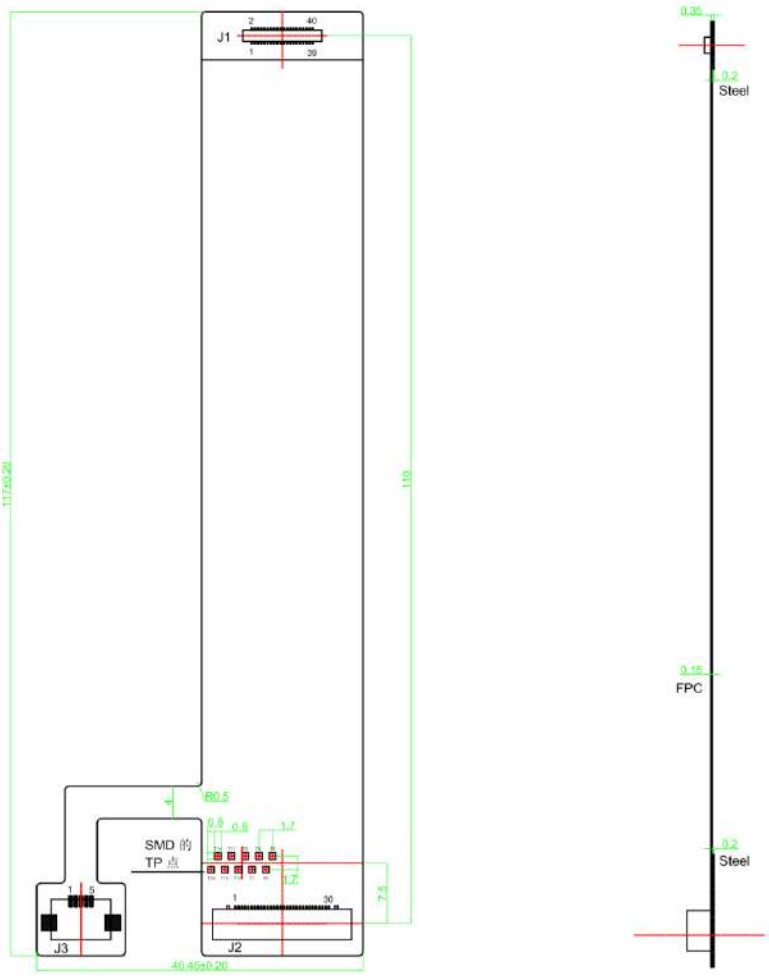
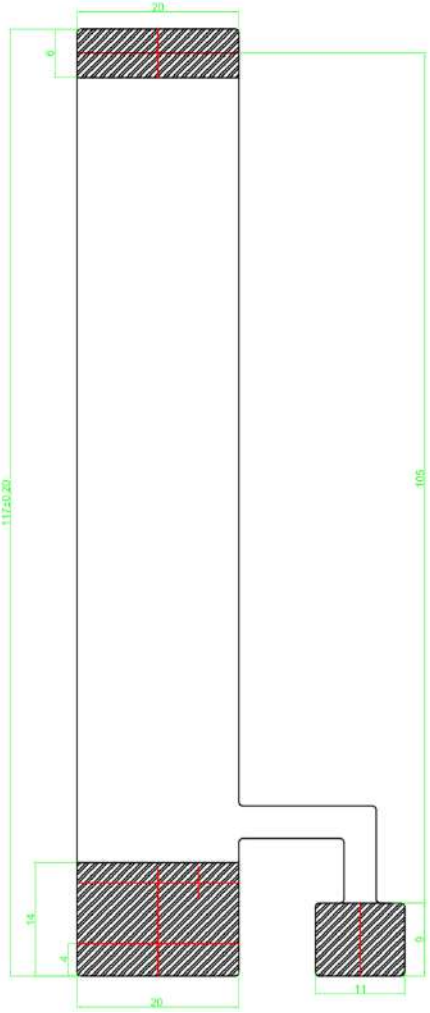
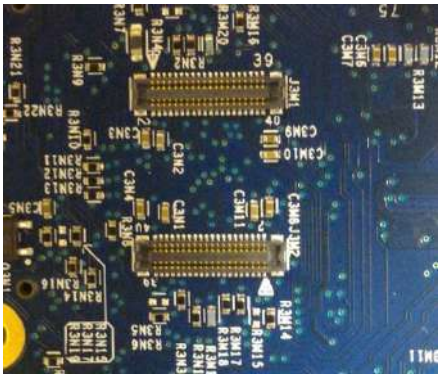
Dimensions (LI-APOLLO-ADP)





Work on Intel Apollo Processor board



Connect pin1 (LI-APOLLO-ADP) to pin1 (Intel Apollo board) … pin40 to pin40

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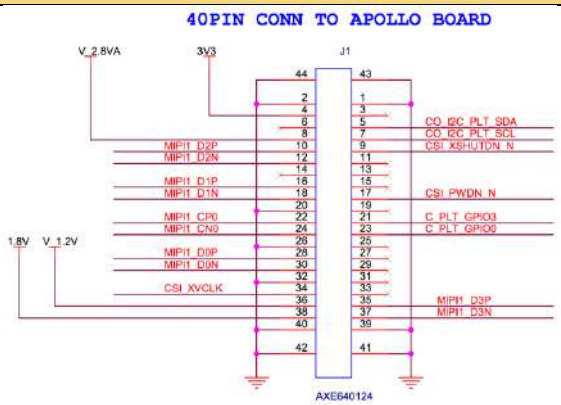
LI-APOLLO-ADP

Interfaces

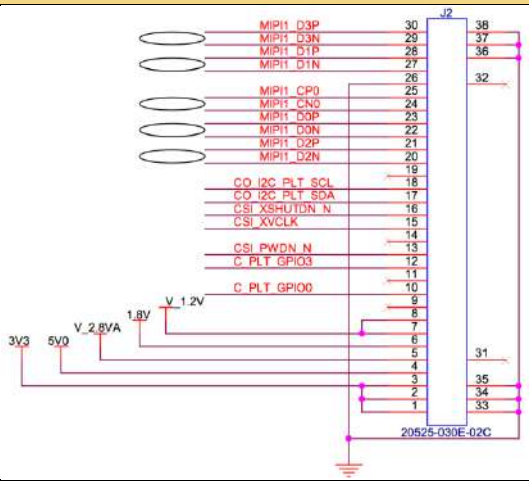
Interface J1

- Part#: AXE640124
- Number of Positions: 40
- Pitch: 0.4mm
- Number of Rows: 2



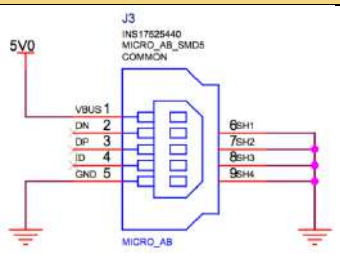
Interface J2

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-01 (100mm)



Interface J3

- Part#: 10118192-0001LF
- Connector Type: USB - micro B
- Number of Contacts: 5
- USB2.0 port for 5V Source



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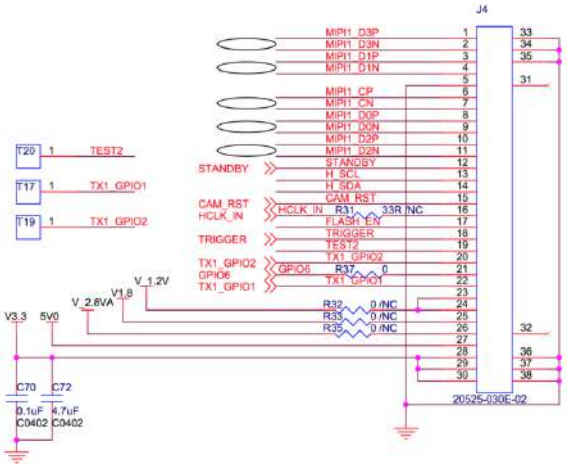
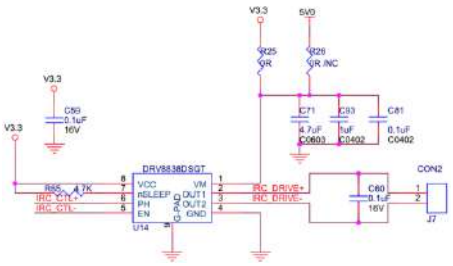
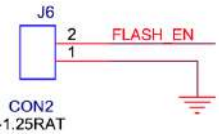
LI-AR023Z-YUV-MIPI

Camera Spec	
Image Sensor	ON Semiconductor AR023Z 1080p HD Sensor
Optical format	1/2.7” (6.6 mm)
Number of active pixels	1928H x 1088V
Pixel size	3.0 um (H) x 3.0 um (V)
Interface	MIPI interface
Lens mount	M12
Weight	12 g
Interfaces	
Interface J4: ▪ Part#: 20525-030E-02C ▪ Number of Positions: 30 ▪ Pitch: 0.4mm ▪ Mating I-PEX cable: FAW-1233	
Interface J7: ▪ Part#: 1734829-2 ▪ Number of Positions: 2 ▪ Pitch: 1.25mm	
Interface J6: ▪ Part#: 1734829-2 ▪ Number of Positions: 2 ▪ Pitch: 1.25mm	

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Absolute Maximum Ratings

Symbol	Definition	Condition	Min	Max	Unit
V_{DD}_MAX	Core digital voltage		–0.3	2.4	V
V_{DD}_IO_MAX	I/O digital voltage		–0.3	4	V
V_{AA}_MAX	Analog voltage		–0.3	4	V
V_{AA}_PIX	Pixel supply voltage		–0.3	4	V
V_{DD}_PLL	PLL supply voltage		–0.3	4	V
VDD_SLVS_MAX	HiSPi I/O digital voltage		–0.3	2.4	V
t_{ST}	Storage temperature		–40	85	°C

Note: Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1080p30 Linear 74MHz Parallel 1.8v

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital operating current	Streaming 1080p30	I_{DD}	1.8		109		mA
I/O digital operating current	Streaming 1080p30	I_{DD_IO}	1.8		16.6		mA
Analog operating current	Streaming 1080p30	I_{AA}	2.8		45		mA
Pixel supply current	Streaming 1080p30	I_{AA_PIX}	2.8		4		mA
PLL supply current	Streaming 1080p30	I_{DD_PLL}	2.8		6.2		mA

Note: Operating currents are measured at the following conditions:
- V_{AA} = V_{AA_PIX} = V_{DD_PLL} = 2.8 V
- V_{DD}= V_{DD_IO} = 1.8 V
- PLL Enabled and PIXCLK = 74.25 MHz
- T_j= 25°C

1080p30 HDR (ALTM) 74MHz Parallel 1.8v

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital operating current	Streaming 1080p30	I_{DD}	1.8		175		mA
I/O digital operating current	Streaming 1080p30	I_{DD_IO}	1.8		18.5		mA
Analog operating current	Streaming 1080p30	I_{AA}	2.8		60.8		mA
Pixel supply current	Streaming 1080p30	I_{AA_PIX}	2.8		4.7		mA
PLL supply current	Streaming 1080p30	I_{DD_PLL}	2.8		6.2		mA

Note: Operating currents are measured at the following conditions:
- V_{AA} = V_{AA_PIX} = V_{DD_PLL} = 2.8 V
- V_{DD}= V_{DD_IO} = 1.8 V
- PLL Enabled and PIXCLK = 74.25 MHz
- T_j = 25°C

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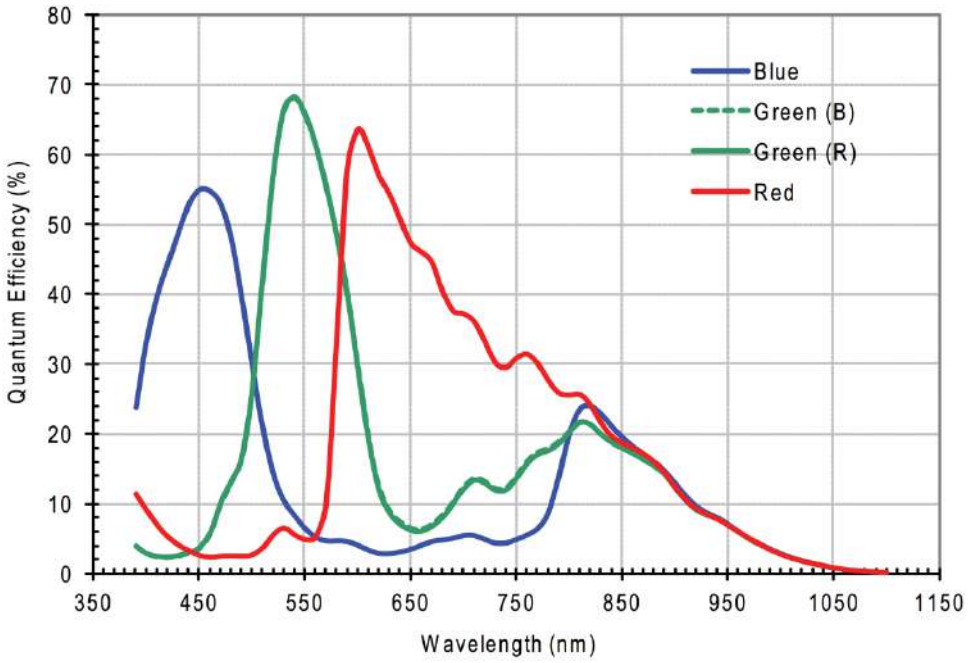
Quantum Efficiency



DC Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.95	V
V_{DD_IO}	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V_{AA}	Analog voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.5	2.8	3.1	V
V_{DD_PLL}	PLL supply voltage		2.5	2.8	3.1	V
V_{DD_SLVS}	HiSPi supply voltage		0.3	0.4	0.6	V
V_{IH}	Input HIGH voltage		V_{DD_IO}*0.7	–	–	V
V_{IL}	Input LOW voltage		–	–	V_{DD_IO}*0.3	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD_IO} or D_{GND}	20	–	–	µA
V_{OH}	Output HIGH voltage		V_{DD_IO}-0.3	–	–	V
V_{OL}	Output LOW voltage		–	–	0.4	V
I_{OH}	Output HIGH current	At specified V_{OH}	-22	–	–	mA
I_{OL}	Output LOW current	At specified V_{OL}	–	–	22	mA

Caution **Stresses greater than those listed in Table 14 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.**

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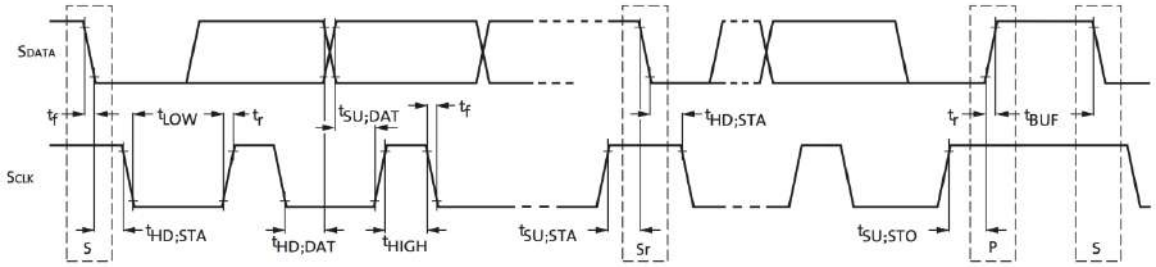
Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Two-Wire Serial Bus Characteristics

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD_IO} = 2.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; T_A = 25°C

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	^{f}SCL	0	100	0	400	KHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	^{t}HD;STA	4.0	-	0.6	-	µs
LOW period of the SCLK clock	^{t}LOW	4.7	-	1.3	-	µs
HIGH period of the SCLK clock	^{t}HIGH	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	^{t}SU;STA	4.7	-	0.6	-	µs
Data hold time	^{t}HD;DAT	0[4]	3.45[5]	0[6]	0.9[5]	µs
Data set-up time	^{t}SU;DAT	250	-	100[6]	-	ns
Rise time of both SDATA and SCLK signals	^{t}r	-	1000	20 + 0.1Cb[7]	300	ns
Fall time of both SDATA and SCLK signals	^{t}f	-	300	20 + 0.1Cb[7]	300	ns
Set-up time for STOP condition	^{t}SU;STO	4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	^{t}BUF	4.7	-	1.3	-	µs
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	CIN_SI	-	3.3	-	3.3	pF
SDATA max load capacitance	CLOAD_SD	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	KΩ

Notes:
1. This table is based on I^{2}C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I^{2}C-compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1V_{DD} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
6. A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

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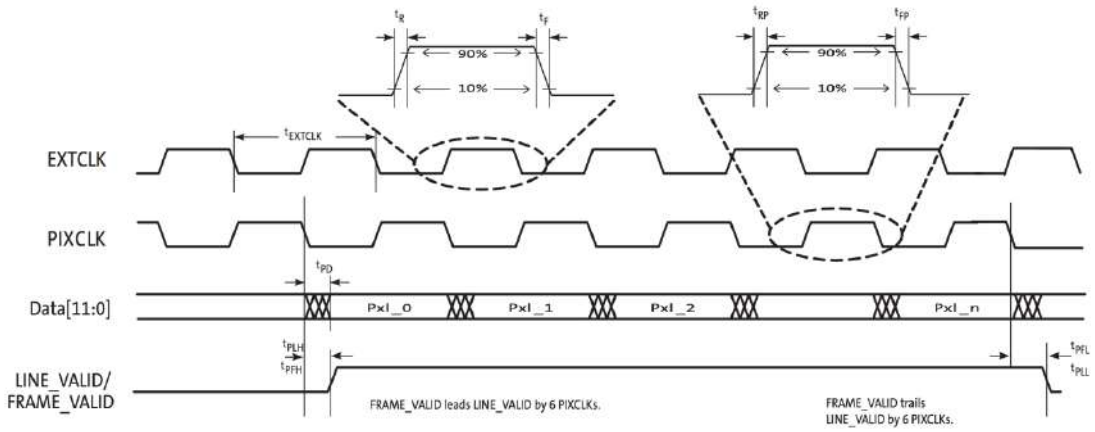
I/O Timing Diagram



I/O Timing Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1s}$	Input clock frequency		6	–	48	MHz
$t_{EXTCLK1}$	Input clock period		20.8	–	166	ns
t_R	Input clock rise time		–	3	–	ns
t_F	Input clock fall time		–	3	–	ns
t_{RP}	Pixclk rise time		–	4	–	ns
t_{FP}	Pixclk fall time		–	4	–	ns
	Clock duty cycle		40	50	60	%
$t_{PIX\ JITTER}$	Jitter on PIXCLK		–	1		ns
t_{CP}	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL Disabled	–	32.4	–	ns
f_{PIXCLK}	PIXCLK frequency	Default, Nominal Voltages	6		74.25	MHz
t_{PD}	PIXCLK to data valid	Default, Nominal Voltages	–	2.3	–	ns
t_{PFH}	PIXCLK to FV HIGH	Default, Nominal Voltages	–	5.7	–	ns
t_{PLH}	PIXCLK to LV HIGH	Default, Nominal Voltages	–	5.5	–	ns
t_{PFL}	PIXCLK to FV LOW	Default, Nominal Voltages	–	4.3	–	ns
t_{PLL}	PIXCLK to LV LOW	Default, Nominal Voltages	–	4.6	–	ns
C_{LOAD}	Output load capacitance		–	<10	–	pF
C_{IN}	Input pin capacitance		–	2.5	–	pF

Note: I/O timing characteristics are measured under the following conditions:
- Temperature is 25°C ambient
- 10 pF load
- 1.8V I/O supply voltage

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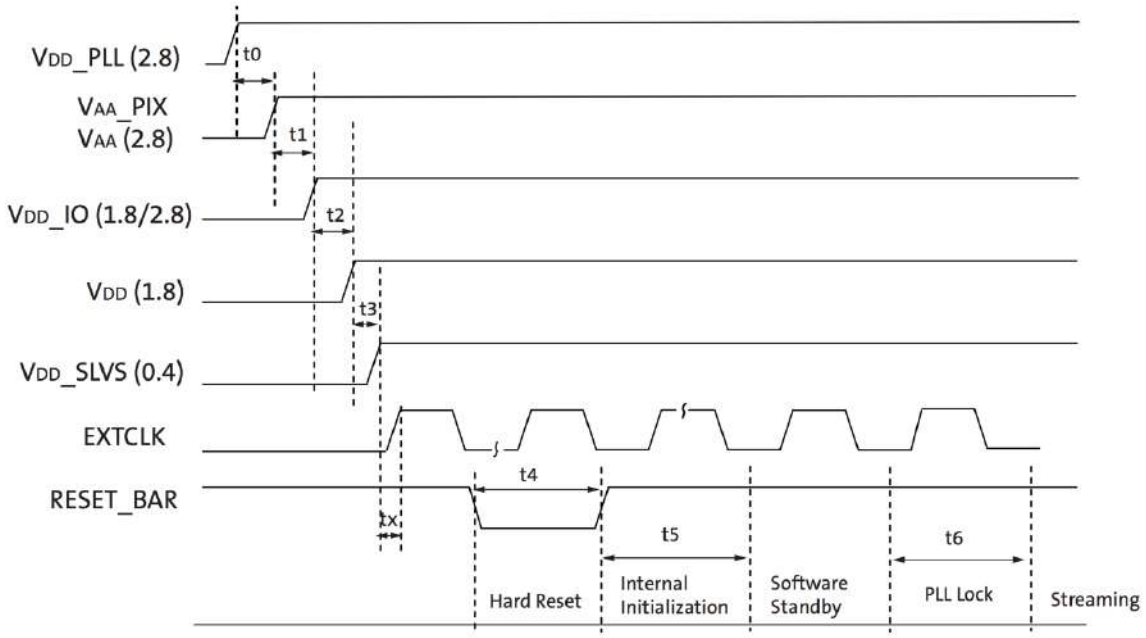
Power Up



Power-Up Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX[3]	t0	0	100	–	µs
VAA/VAA_PIX to VDD_IO	t1	0	100	–	µs
VDD_IO to VDD	t2	0	100	–	µs
VDD to VDD_SLVS	t3	0	100	–	µs
Xtal settle time	tx	–	30[1]	–	ms
Hard Reset	t4	1[2]	–	–	ms
Internal Initialization	t5	150000	–	–	EXTCLKs
PLL Lock Time	t6	1	–	–	ms

Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that VDD_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.

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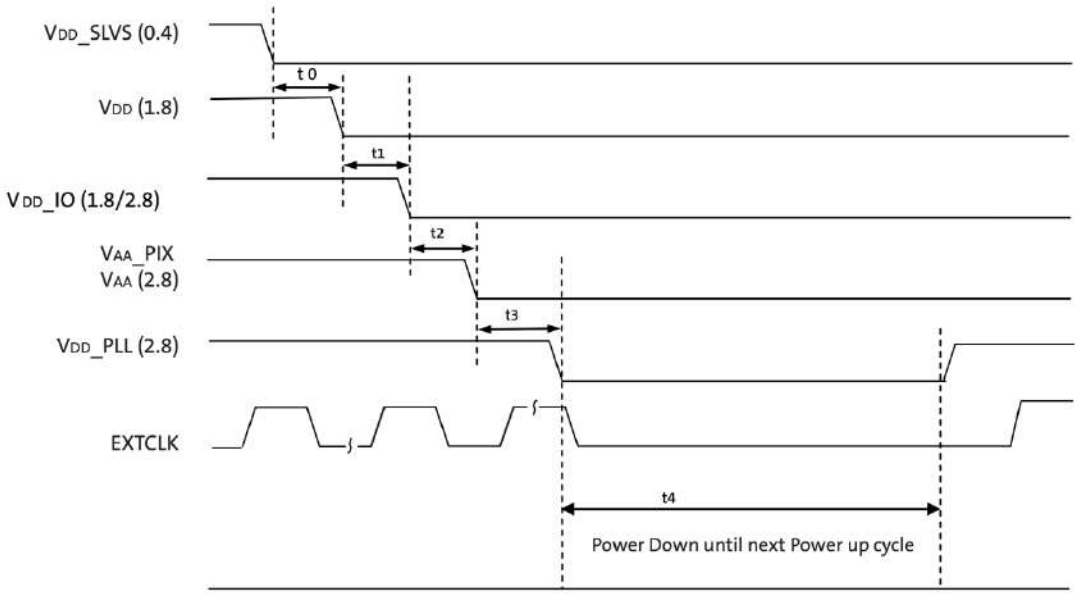
Power Down



Power-Down Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_SLVS to VDD	t0	0	–	–	µs
VDD to VDD_IO	t1	0	–	–	µs
VDD_IO to VAA/VAA_PIX	t2	0	–	–	µs
VAA/VAA_PIX to VDD_PLL	t3	0	–	–	µs
PwrDn until Next PwrUp Time	t4	100	–	–	ms

t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

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